REMARKS

Claims 1-20 are pending. Claims 1-20 are rejected. No claims are amended herein.

112 Rejection

Claim 9 is rejected under 35 USC 112 second paragraph, as being indefinite for failing to particularly point out and distinctly claim the invention. Specifically, the Examiner contends that the Claim 9 recitation "respective cache unit" is unclear because its relationship to previously recited cache units is not "positively" recited (outstanding Office Action, page 2). The Applicants respectfully disagree with the Examiner's contentions regarding Claim 9. Claim 1 includes a limitation that is drawn to a "plurality of cache units." The limitation "respective cache unit" of Claim 9 is merely intended to refer to one of the plurality of cache units that are recited in Claim 1 (from which Claim 9 depends). This usage of the term "respective" represents a usage of the term that is consistent with that which is commonly accepted. Therefore, the Applicants respectfully request the withdrawal of the rejection of Claim 9 and under 35 U.S.C. 112 second paragraph.

102 Rejection

Claims 1-4, 7 and 9 are rejected under 35 U.S.C. § 102(e) as being anticipated by (U.S. Patent No. 6,587,926). The Applicants have reviewed the cited reference and respectfully submit that the present invention as recited in Claims 1-4, 7 and 9 are neither anticipated nor rendered obvious by Arimilli et al.

The Examiner is respectfully directed to independent Claim 1 that sets forth that an embodiment of the present invention includes a cache coherent multiple processor integrated circuit comprising:

> ...an embedded RAM unit for storing instructions and data for the processor units; a cache coherent bus coupled to the processor units and the embedded RAM unit, the bus configured to provide cache coherent snooping commands from the processor units to ensure

cache coherency between the cache units for the processors and the embedded RAM unit.

Claims 2-4, 7 and 9 depend from Claim 1 and recite additional features of the Claimed invention.

Arimilli et al. does not anticipate or render obvious a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in claim 1. Arimilli et al. only shows a method and system for managing a data access transaction within a hierarchical data storage system. The Examiner indicated in the outstanding Office Action that the aforementioned limitation of Claim 1 is readable on matter taught by Arimilli et al. at column 2, lines 1-5. In the referenced passage, it is disclosed that some prior art systems allow devices snooping a system bus to identify and properly route bus transactions by including an address tag that identifies a request source in each data access request and by subsequently returning the address tag with each corresponding response. The Applicants' respectfully submit that a fair reading of the referenced passage shows that Arimilli et al. is primarily concerned with managing the routing of data access transactions and is silent a teaching or suggestion that anticipates or renders obvious a bus that is configured to provide cache coherent snooping commands that maintain cache coherency between processor cache units and a RAM unit. Indeed, nowhere in the Arimilli et al. reference is a bus that is configured to provide cache coherent snooping commands from processor units that ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in claim 1. Consequently, Arimilli et al. does not anticipate or render obvious the embodiment of the Applicants' invention set forth in Claim 1.

The Examiner is reminded that in order to anticipate a claim a reference must teach each and every element of the Claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art

reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed Cir. 1987). It is clear from the discussion above that "each and every element" of Claim 1 is in fact not described by the Arimilli et al. reference. Arimilli et al. does not "either expressly or inherently" show or suggest a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in claim 1.

Accordingly, Applicants respectfully submit that Arimilli et al. does not anticipate or render obvious the present claimed invention as is recited in Claims 2-4, 7 and 9 dependent on Claim 1 and that these Claims overcome the rejection under 35 U.S.C. 102(e) as being dependent on an allowable base claim.

Claim 5 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Arimilli et al. (U.S. Patent No. 6,571,322). Arimilli et al. (U.S. Patent No. 6,571,322) does not overcome the shortcomings of Arimilli et al. (U.S. Patent No. 6,587,926) noted above. Arimilli et al. (U.S. Patent No. 6,571,322) does not anticipate or render obvious a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in claim 1 (from which Claim 5 depends). Arimilli et al. (U.S. Patent No. 6,571,322) only shows a multiprocessor computer system with a mechanism for cache intervention. Nowhere in the Arimilli et al. (U.S. Patent No. 6,571,322) reference is a bus that is configured to provide cache coherent snooping commands from processor units that ensure cache coherency between the cache units for the processor units and an embedded RAM unit

taught or suggested as is recited in claim 1 (from which Claim 5 depends). Consequently, Arimilli et al. (U.S. Patent No. 6,587,926) either alone or in combination with Arimilli et al. (U.S. Patent No. 6,571,322) does not anticipate or render obvious the embodiment of Applicants' invention as set forth in Claim 1 (from which Claim 5 depends).

Accordingly, Applicants respectfully submit that Arimilli et al. (U.S. Patent No. 6,587,926) alone or in combination with Arimilli et al. (U.S. Patent No. 6,571,322) does not anticipate or render obvious the present claimed invention as is recited in Claim 5 dependent on Claim 1 and that Claim 5 overcomes the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

Claim 6 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Miller (U.S. Patent No. 6,560,682). Miller et al. does not overcome the shortcomings of Arimilli et al. noted above. Miller et al. does not anticipate or render obvious a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in claim 1 (from which Claim 6 depends). Miller et al only shows a system and method for terminating lock-step sequences in multiprocessor systems. Nowhere in the Miller et al. reference is a bus that is configured to provide cache coherent snooping commands from processor units that ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in claim 1 (from which Claim 6 depends). Consequently, Arimilli et al. either alone or in combination with Miller et al. does not anticipate or render obvious the Applicants invention as set forth in Claim 1 (from which Claim 6 depends).

Accordingly, Applicants respectfully submit that Arimilli et al. (U.S. Patent No. 6,587,926) alone or in combination with Miller et al. (U.S. Patent No. 6,560,682) does not anticipate or render obvious the present claimed invention as is recited in Claim 6 dependent on Claim 1 and that Claim 6 overcomes the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Bitar et al. (U.S. Patent No. 6,418,460). Bitar et al. does not overcome the shortcomings of Arimilli et al. noted above. Bitar et al. does not anticipate or render obvious a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in claim 1 (from which Claim 8 depends). Bitar et al. only shows a system and method for finding preempted threads in a multi-threaded application. Nowhere in the Bitar et al. reference is a bus that is configured to provide cache coherent snooping commands from processor units that ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in claim 1 (from which Claim 8 depends). Consequently, Arimilli et al. either alone or in combination with Bitar et al., does not anticipate or render obvious the Applicants' invention as set forth in Claim 1 (from which Claim 8 depends).

Accordingly, Applicants respectfully submit that Arimilli et al. (U.S. Patent No. 6,587,926) alone or in combination with Bitar et al. (U.S. Patent No. 6,418,460) does not anticipate or render obvious the present claimed invention as is recited in Claim 8 dependent

on Claim 1 and that Claim 8 overcomes the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

Claims 10-13, 16 and 18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Sherburne (U.S. Patent Application Publication No. 2002/0184546). Sherburne does not overcome the shortcomings of Arimilli et al. noted above. Sherburne does not anticipate or render obvious a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in claim 10. Sherburne only shows a method and device for modifying the contents of memory. Nowhere in the Sherburne et al. reference is a bus that is configured to provide cache coherent snooping commands from processor units that ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in claim 10. Consequently, Arimilli et al. either alone or in combination with Sherburne does not anticipate or render obvious the Applicants' invention as set forth in Claim 10.

Accordingly, Applicants respectfully submit that Arimilli et al. alone or in combination with Sherburne does not anticipate or render obvious the present claimed invention as is recited in Claims 11-13, 16 and 18 dependent on Claim 10 and that these Claims overcome the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

Claim 14 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Arimilli et al. (U.S. Patent No. 6,571,322). Arimilli et al. (U.S. Patent No. 6,571,322) does not overcome the shortcomings of Arimilli et al. (U.S.

Patent No. 6,587,926) noted above. Arimilli et al. (U.S. Patent No. 6,571,322) does not anticipate or render obvious a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in claim 10 (from which Claim 14 depends). Arimilli et al. (U.S. Patent No. 6,571,322) only shows a multiprocessor computer system with a mechanism for cache intervention. Nowhere in the Arimilli et al. (U.S. Patent No. 6,571,322) reference is a bus that is configured to provide cache coherent snooping commands from processor units that ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in claim 10 (from which Claim 14 depends). Consequently, Arimilli et al. (U.S. Patent No. 6,587,926) either alone or in combination with Arimilli et al. (U.S. Patent No. 6,571,322) does not anticipate or render obvious the Applicants' invention as set forth in Claim 10 (from which Claim 14 depends).

Accordingly, Applicants respectfully submit that Arimilli et al. (U.S. Patent No. 6,587,926) alone or in combination with Arimilli et al. (U.S. Patent No. 6,571,322) does not anticipate or render obvious the present claimed invention as is recited in Claim 14 dependent on Claim 10 and that Claim 14 overcomes the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Miller et al. (U.S. Patent No. 6,560,682). Miller et al. does not overcome the shortcomings of Arimilli et al. noted above. Miller et al. does not anticipate or render obvious a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor

units to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in claim 10 (from which Claim 15 depends). Miller et al. only shows a system and method for terminating lock-step sequences in multiprocessor systems. Nowhere in the Miller et al. reference is a bus that is configured to provide cache coherent snooping commands from processor units that ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in claim 10 (from which Claim 15 depends). Consequently, Arimilli et al. either alone or in combination with Miller et al. does not anticipate or render obvious the Applicants invention as set forth in Claim 10 (from which Claim 15 depends).

Accordingly, Applicants respectfully submit that Arimilli et al. (U.S. Patent No. 6,587,926) alone or in combination with Miller et al. (U.S. Patent No. 6,560,682) does not anticipate or render obvious the present claimed invention as is recited in Claim 15 dependent on Claim 10 and that Claim 15 overcomes the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

Claim 17 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Miller et al. (U.S. Patent No. 6,560,682). Miller et al. does not overcome the shortcomings of Arimilli et al. noted above. Miller et al. does not anticipate or render obvious a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in claim 10 (from which Claim 17 depends). Miller et al. only shows a system and method for terminating lock-step sequences in multiprocessor systems. Nowhere in the Miller et al. reference is a bus that is configured to provide cache coherent

snooping commands from processor units that ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in claim 10 (from which Claim 17 depends). Consequently, Arimilli et al. either alone or in combination with Miller et al. does not anticipate or render obvious the Applicants invention as set forth in Claim 10 (from which Claim 17 depends).

Accordingly, Applicants respectfully submit that Arimilli et al. (U.S. Patent No. 6,587,926) alone or in combination with Miller et al. (U.S. Patent No. 6,560,682) does not anticipate or render obvious the present claimed invention as is recited in Claim 17 dependent on Claim 10 and that Claim 17 overcomes the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

Claims 19 and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Arimilli et al. (U.S. Patent No. 6,571,322). Arimilli et al. (U.S. Patent No. 6,571,322) does not overcome the shortcomings of Arimilli et al. (U.S. Patent No. 6,587,926) noted above. Arimilli et al. (U.S. Patent No. 6,571,322) does not anticipate or render obvious a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in claim 19. Arimilli et al. (U.S. Patent No. 6,571,322) only shows a multiprocessor computer system with a mechanism for cache intervention. Nowhere in the Arimilli et al. (U.S. Patent No. 6,571,322) reference is a bus that is configured to provide cache coherent snooping commands from processor units that ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in claim 19. Consequently, Arimilli et al. (U.S.

Patent No. 6,587,926) either alone or in combination with Arimilli et al. (U.S. Patent No. 6,571,322) does not anticipate or render obvious the Applicants invention as set forth in Claim 19.

Accordingly, Applicants respectfully submit that Arimilli et al. (U.S. Patent No. 6,587,926) alone or in combination with Arimilli et al. (U.S. Patent No. 6,571,322) does not anticipate or render obvious the present claimed invention as is recited in Claim 20 dependent on Claim 19 and that Claim 20 overcomes the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

Conclusion

In light of the above-listed amendments and remarks, Applicants respectfully request allowance of the remaining Claims.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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